NCP1523

3 MHz, 600 mA, High-Efficiency, Adjustable Output Voltage Stepdown Converter

The NCP1523 stepdown PWM DC−DC converter is optimized for portable applications powered from 1−cell Li−ion or 3−cell Alkaline/NiCd/NiMH batteries. The device is available in an adjustable output voltage from 0.9 V to 2.3 V. It uses synchronous rectification to increase efficiency and reduce external part count. The device also has a built−in 3 MHz (nominal) oscillator which reduces component size by allowing a small inductor and capacitors. Automatic switching PWM/PFM mode offers improved system efficiency.

Finally, it includes an integrated soft−start, cycle−by−cycle current limiting, and thermal shutdown protection. The NCP1523 is available in a space saving, 8 pin chip scale package.

Features

- Up to 93% Efficiency
- Sources up to 600 mA
- 3 MHz Switching Frequency
- Adjustable Output Voltage from 0.9 V to 2.3 V
- 60 μA Quiescent Current
- Synchronous Rectification for Higher Efficiency.
- 2.7 V to 5.5 V Input Voltage Range
- Thermal Limit Protection
- Shutdown Current Consumption of 0.3 μA
- This is a Pb−Free Device*

Typical Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment

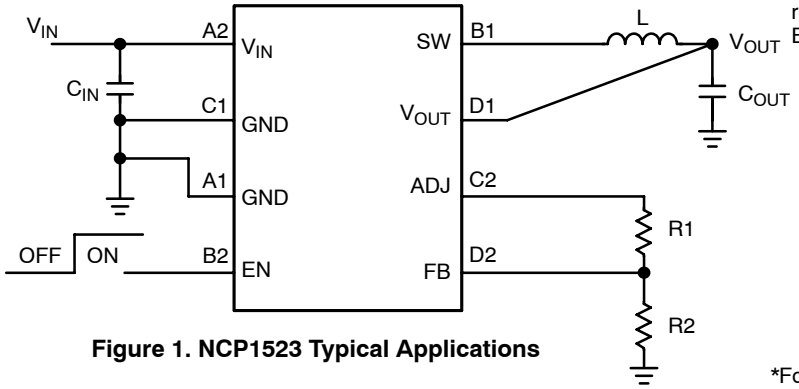


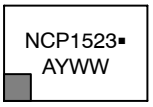
Figure 1. NCP1523 Typical Applications

ON Semiconductor®

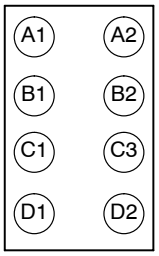
http://onsemi.com

MARKING DIAGRAM

FLIP−CHIP−8
CASE 766AE



A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package



Top View
(Bumps Below)

PIN: A1 − GND
A2 − V_{IN}
B1 − SW
B2 − EN
C1 − GND
C2 − ADJ
D1 − V_{OUT}
D2 − FB

ORDERING INFORMATION

Device	Package	Shipping†
NCP1523FCT2G	FLIP−CHIP−8 (Pb−Free)	3000 / Tape * Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

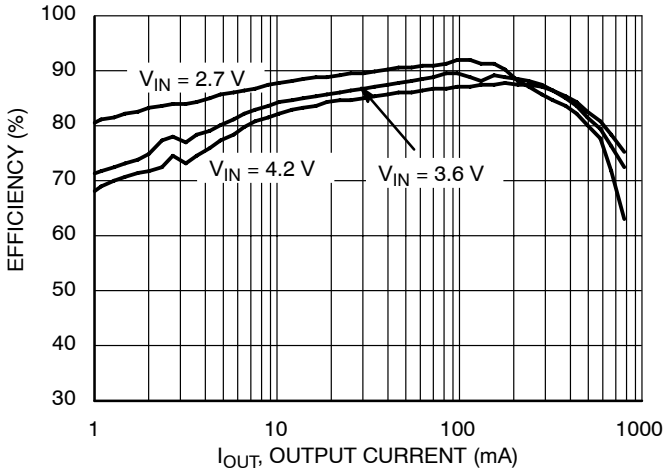


Figure 2. Efficiency vs. Output Current (V_{OUT} = 2.0 V, Temperature = 25°C)

TYPICAL APPLICATIONS

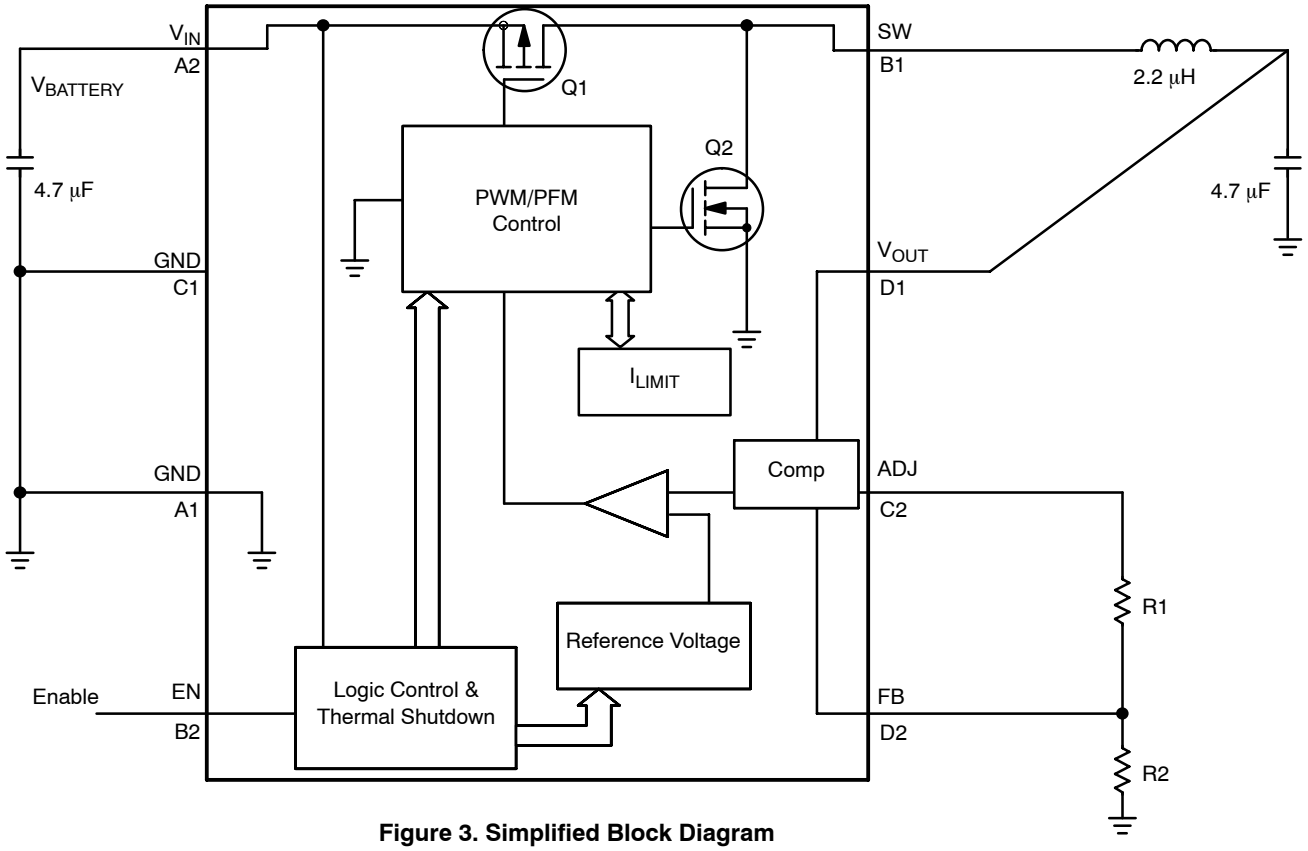


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1	GND	Power Ground	Ground connection for the NFET Power Stage and the analog sections.
B2	V_{IN}	Power Input	Power Supply Input for the PFET Power stage and the Analog Sections of the IC.
B1	S_W	Analog Output	Connection from Power MOSFETs to the Inductor.
B2	EN	Digital Input	Enable for Switching Regulator. This pin is active high. This pin contains an internal pulldown resistor.
C1	GND	Power Ground	Ground connection for the NFET Power Stage and the analog sections.
C2	ADJ	Analog Input	This pin is the compensation input. R1 is connected to this pin.
D1	V_{OUT}	Analog Input	This pin is connected of the converter's output. This is the sense of the output voltage.
D2	F_B	Analog Input	Feedback voltage from the output of the power supply. This is the input to the error amplifier.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{MIN}	−0.3	V
Maximum Voltage All Pins (Note 1)	V_{MAX}	7	V
Maximum Voltage Enable, FB, SW	V_{MAX}	V_{IN} + 0.3	V
Thermal Resistance, Junction−to−Air (Note 2)	R_{JA}	159	°C/W
Operating Ambient Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Junction Operating Temperature	T_J	−40 to 125	°C
Latchup Current maximum Rating T_A = 85°C (Note 4)	L_U	±100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	V_{ESD}	 2.0 200	 kV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22−A108B
2. For the 8−Pin Chip scale package, the R_{JA} is highly dependent of the PCB heatsink area. R_{JA} = 159°C/W with 50 mm^2 PCB heatsink area.
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115
4. Latchup current maximum rating per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS

(Typical values are referenced to T_A = +25°C, Minimum and Maximum values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions V_{IN} = 3.6 V, V_{OUT} = 1.8 V unless otherwise noted)

Symbol	Rating	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	2.7		5.5	V
V_{UVLO}	Under voltage Lockout (V_{IN} Falling)		2.4		V
I_q	Quiescent Current PFM no load		 60	 95	μA
I_{STB}	Standby Current, EN Low		0.3	1.2	μA
F_{OSC}	Oscillator Frequency	2.400	3	3.600	MHz
I_{LIM}	Peak Inductor Current		1200		mA
V_{REF}	Feedback Reference Voltage		0.6		V
V_{FBtol}	F_B Pin Tolerance Overtemperature	−3		3	%
ΔV_{FB}	Reference Voltage Line Regulation		0.1		%
V_{OUT}	Output Voltage Accuracy (Note 5)	−3%	V_{nom}	+3%	V
V_{OUT}	Minimum Output Voltage		0.9		V
V_{OUT}	Maximum Output Voltage		2.3		V
ΔV_{OUT}	Output Voltage Line Regulation (V_{IN} = 2.7 − 5.5) I_O = 100 mA		0.1		%
$V_{LOA-DREG}$	Voltage Load Regulation (I_O = 150 mA to 300 mA) (I_O = 150 mA to 600 mA)		 0.0005 0.001		 %/mA %/mA
	Duty Cycle			100	%
R_{SWH}	P−Channel On−Resistance		300		mΩ
R_{SWL}	N−Channel On−Resistance		300		mΩ
I_{LeakH}	P−Channel Leakage Current		0.05		μA
I_{LeakL}	N−Channel Leakage Current		0.01		μA
V_{ENH}	Enable Pin High	1.2			V
V_{ENL}	Enable Pin Low			0.4	V
T_{START}	Soft−Start Time		350	450	μs

5. The overall output voltage tolerance depends upon the accuracy of the external resistor (R1, R2).

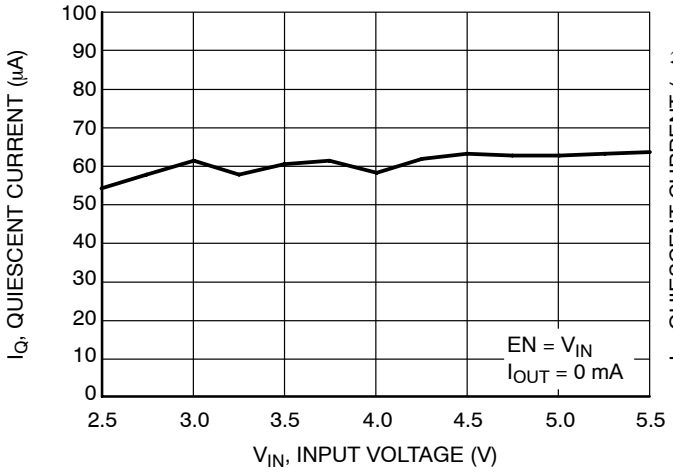


Figure 4. Quiescent Current vs. Supply Voltage

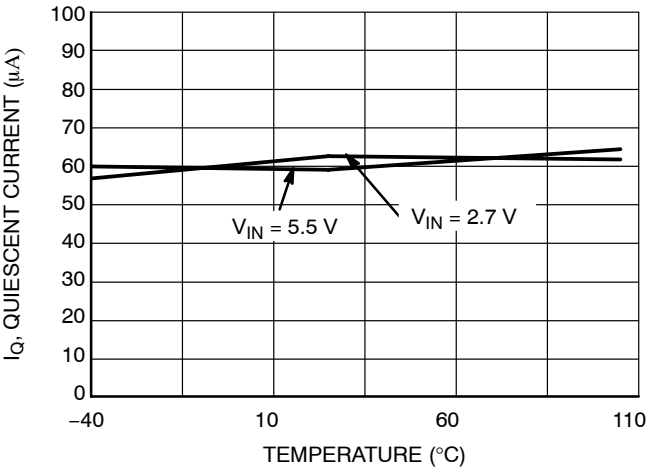


Figure 5. Quiescent Current vs. Temperature

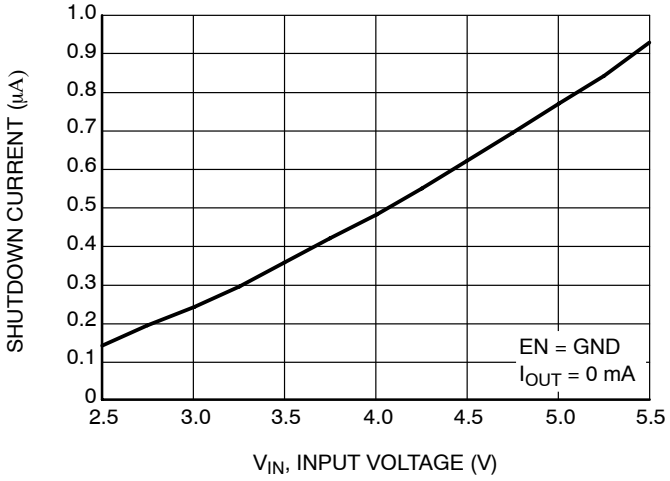


Figure 6. Shutdown Current vs. Supply Voltage

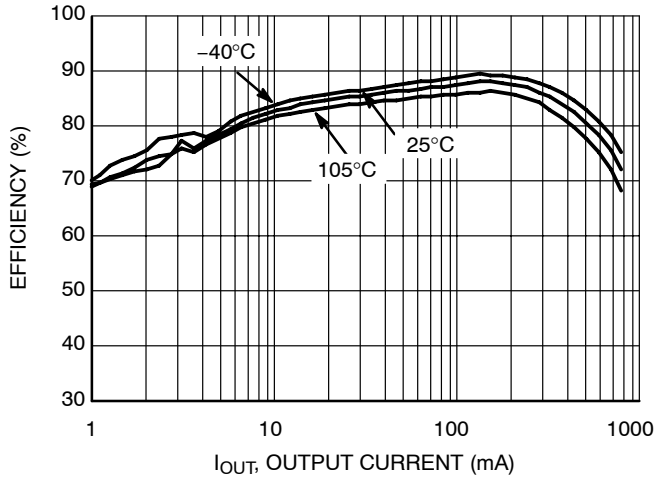


Figure 7. Efficiency vs. Output Current (V_{OUT} = 1.8 V, V_{IN} = 3.6 V)

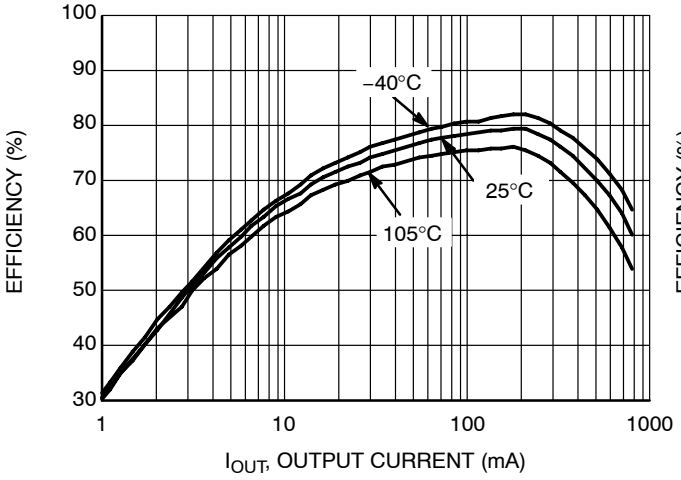


Figure 8. Efficiency vs. Output Current (V_{OUT} = 0.9 V, V_{IN} = 3.6 V)

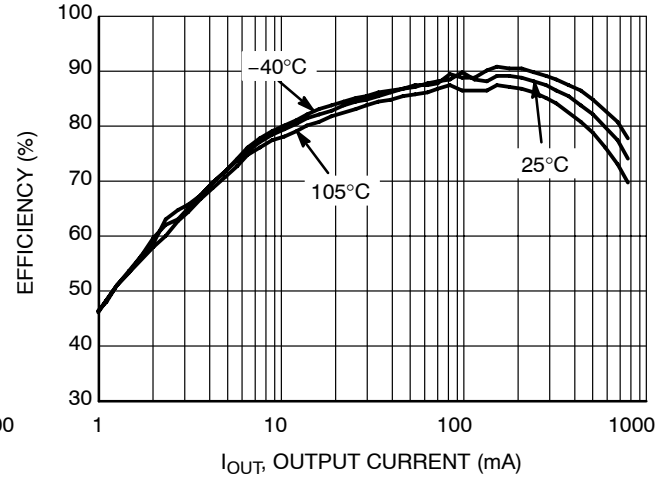


Figure 9. Efficiency vs. Output Current V_{OUT} = 2.0 V, V_{IN} = 3.6 V)

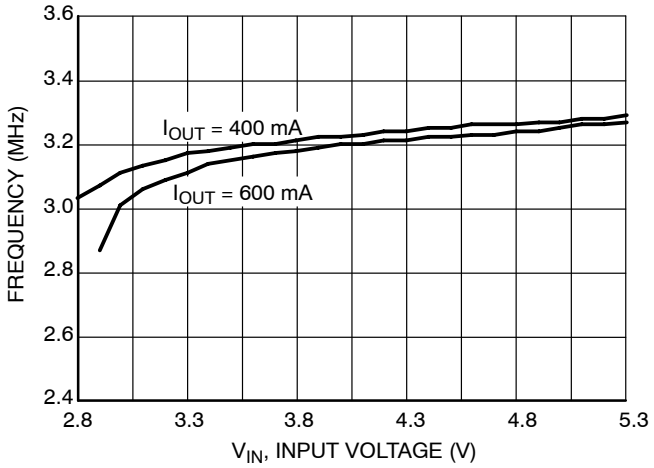


Figure 10. Frequency vs. Input Voltage

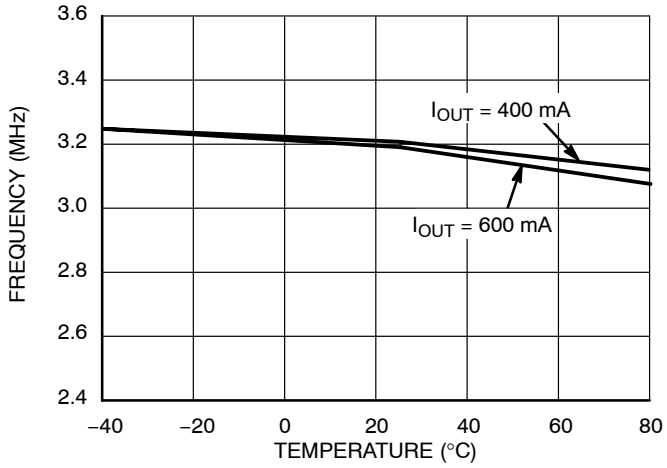


Figure 11. Frequency vs. Temperature

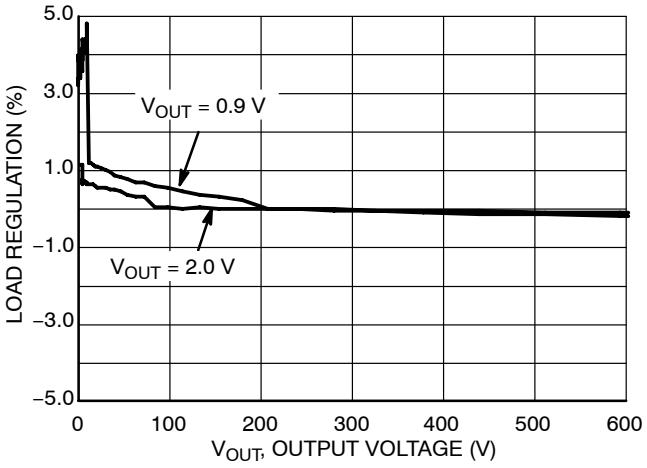


Figure 12. Load Regulation

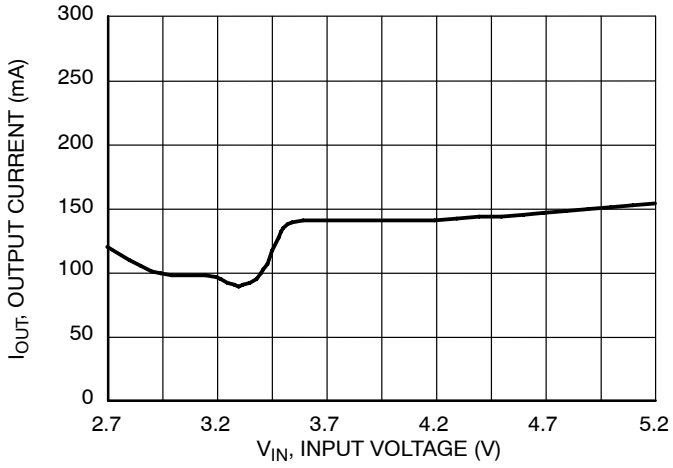


Figure 13. PFM/PWM Threshold vs. Input Voltage

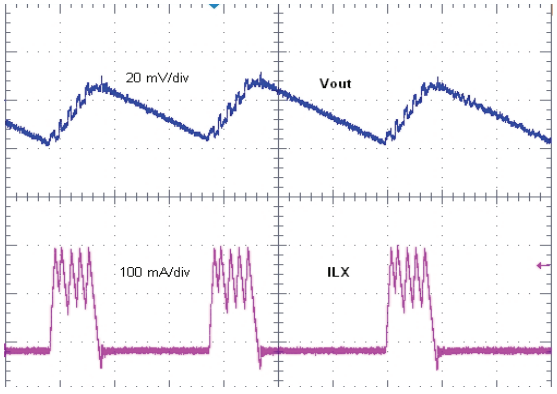


Figure 14. Stepdown Converter PFM Mode Operation

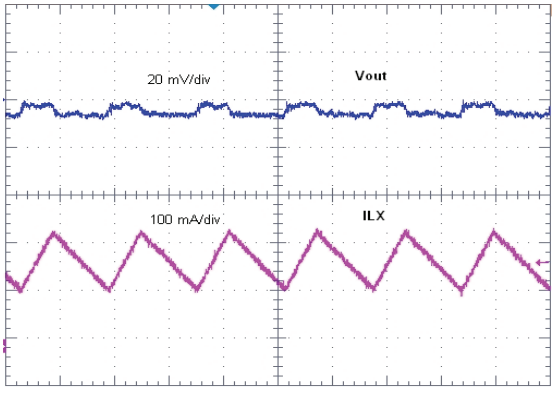


Figure 15. Stepdown Converter PWM Mode Operation

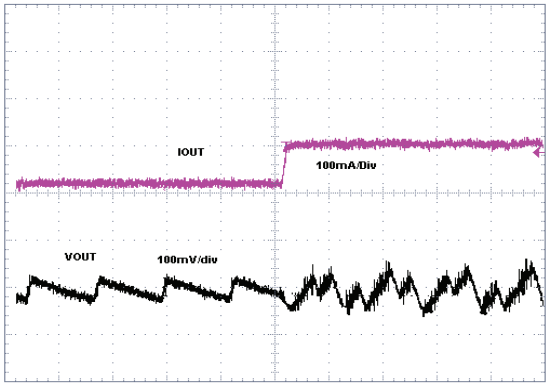


Figure 16. Load Transient Response in PFM Operation (10 mA to 100 mA)

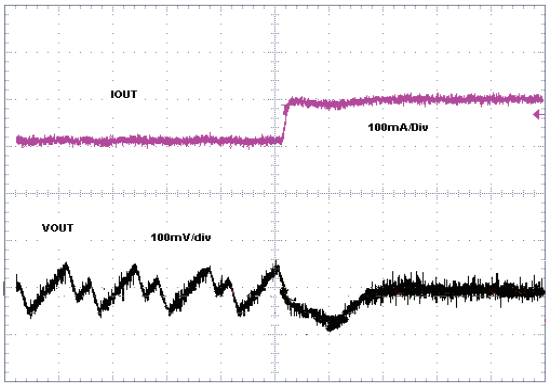


Figure 17. Load Transient Response Between PFM and PWM Operation (100 mA to 200 mA)

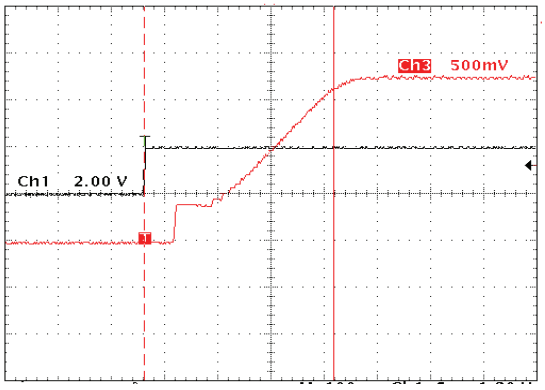


Figure 18. Soft−Start Time (V_{IN} = 3.6 V)

OPERATION DESCRIPTION

Overview

The NCP1523 uses a constant frequency, voltage mode stepdown architecture. Both the main (P−Channel MOSFET) and synchronous (N−Channel MOSFET) switches are internal.

It delivers a constant voltage from either a single Li−Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDA. The output voltage is sets by external resistor divider. The NCP1523 sources up to 600 mA depending on external components chosen.

The NCP1523 works with two mode of operation PWM/PFM depending on the current required. The device operates in PWM mode at load currents of approximately 130 mA or higher, having voltage tolerance of ±3% with 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM mode for reduced current consumption (I_Q = 60 μA typ) and a longer battery life.

Additional features include soft−start, under voltage protection, current overload protection, and thermal shutdown protection. As shown in Figure 1, only six external components are required for implementation. The part uses an internal reference voltage of 0.6 V. It is recommended to keep the part in shutdown until the input voltage is 2.7 V or higher.

PWM Operating Mode

In this mode, the output voltage of the NCP1523 is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed frequency of 3 MHz. The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the PWM ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error voltage amplifier. Once this has occurred, the PWM comparator resets the flip−flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

PFM Operating Mode

Under light load conditions, The NCP1523 enters in low current PFM mode operation to reduce power consumption. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PM comparator (typically V_{nom} − 2%), a new cycle will be initiated by the PM comparator to turn on the switch Q1. Q1 remains ON until the peak inductor current reaches 200 mA (nom). Then I_{LIM} comparator goes high to switch off Q1. After a short dead time delay, switch rectifier Q2 is turn ON. The Negative current detector (NCD) will detect when the inductor current drops below zero and send the signal to turn off Q2. The output voltage continues to decrease through discharging the output capacitor. When the output voltage falls below the threshold of the PFM comparator, a new cycle starts immediately.

Cycle−by−Cycle Current Limitation

From the block diagram (Figure 3), an I_{LIM} comparator is used to realize cycle−by−cycle current limit protection. The comparator compares the SW pin voltage with the reference voltage, which is biased by a constant current. If the inductor current reaches the limit, the I_{LIM} comparator detects the SW voltage falling below the reference voltage and releases the signal to turn off the switch Q1. The cycle−by−cycle current limit is set at 1200 mA (nom).

Soft−Start

The NCP1523 uses soft−start to limit the inrush current when the device is initially powered up or enabled. Soft−start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft−start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Shutdown Mode

When the EN pin has a voltage applied of less than 0.4 V, the NCP1523 will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.3 μA (typical value). Applying a voltage above 1.2 V to EN pin will enable the device for normal operation. The device will go through soft−start to normal operation. EN pin should be activated after the input voltage is applied.

Thermal Shutdown

circuitry is provided to protect the integrated circuit in the event that the maximum junction Temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating and it is not intended as a substitute for proper heatsinking.

APPLICATION INFORMATION

Output Voltage Selection

The output voltage is programmed through an external resistor divider connected from ADJ to FB then to GND. For low power consumption and noise immunity, the resistor from FB to GND (R2) should be in the [100 kΩ – 600 kΩ] range. If R2 is 200 kΩ given the V_{FB} is 0.6 V, the current through the divider will be 3 μA.

The formula below gives the value of V_{OUT}, given the desired R1 and the R1 value,

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 1)}$$

- V_{OUT}: output voltage (volts)
- V_{FB}: feedback voltage = 0.6 V
- R1: feedback resistor from V_{OUT} to FB
- R2: feedback resistor from FB to GND

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is I_O, max/2.

For NCP1523, a low profile ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V_{IN} Pin.

Table 1. LIST OF INPUT CAPACITOR

Murata	GRM188R60J475KE
	GRM21BR71C475KA
Taiyo Yuden	JMK212BY475MG
TDK	C2012X5ROJ475KB
	C1632X5ROJ475KT

Output L–C Filter Design Considerations:

The NCP1523 is built in 3 MHz frequency and uses voltage mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L–C filter must be selected to work with internal compensation. For NCP1523, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 4.7 μF

The corner frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{out}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 4.7\ \mu F}} = 49.5\ kHz \quad \text{(eq. 2)}$$

The device operates with inductance value between 1 μH and maximum of 4.7 μH.

If the corner frequency is moved, it is recommended to check the loop stability depending of the output ripple voltage accepted and output current required. For lower frequency, the stability will be increase; a larger output capacitor value could be chosen without critical effect on the system. On the other hand, a smaller capacitor value increases the corner frequency and it should be critical for the system stability. Take care to check the loop stability. The phase margin is usually higher than 45°.

Table 2. L–C FILTER EXAMPLE

Inductance (L)	Output Capacitor (C_{OUT})
1 μH	10 μF
2.2 μH	4.7 μF
4.7 μH	2.2 μF

Inductor Selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (Δ_{IL}) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 3)}$$

Δ_{IL} peak to peak inductor ripple current

L inductor value

f_{SW} Switching frequency

The Saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2} \quad \text{(eq. 4)}$$

$I_{L(MAX)}$ Maximum Inductor Current

$I_{O(MAX)}$ Maximum Output Current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 3. LIST OF INDUCTOR

FDK	MIPW3226 Series
TDK	VLF3010AT Series
Taiyo Yuden	LQ CBL2012
Coil Craft	DO1605–T Series
	LPO3010

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{4 \times f_{SW} \times C_{OUT}} + ESR \right) \quad \text{(eq. 5)}$$

In PFM mode (at light load), the output voltage is regulated by pulse frequency modulation. The output voltage ripple is independent of the output capacitor value. It is set by the threshold of PM comparator.

Table 4. LIST OF OUTPUT CAPACITOR ROHS

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR71C475KA	
	GRM188R60OJ106ME	10 μF
Taiyo Yuden	JMK212BY475MG	4.7 μF
	JMK212BJ106MG	10 μF
TDK	C2012X5ROJ475KB	4.7 μF
	C1632X5ROJ475KT	
	C2012X5ROJ106K	10 μF

APPLICATION BOARD

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

1. Use star−ground connection to connect the IC ground nodes and capacitor GND nodes together at one point. Keep them as close as possible, and then connect this to the ground plane through several vias. This will reduce noise in the ground plane by preventing the switching currents from flowing through the ground plane.
2. Place the power components (i.e., input capacitor, inductor and output capacitor) as close together as possible for best performance. All connecting traces must be short, direct, and wide to reduce voltage errors caused by resistive losses through the traces.
3. Separate the feedback path of the output voltage from the power path. Keep this path close to the NCP1523 circuit. And also route it away from noisy components. This will prevent noise from coupling into the voltage feedback trace.
4. Place the DC−DC converter away from noise sensitive circuitry, such as RF circuits.

The following shows the NCP1523 demo board schematic and layout and bill of materials:

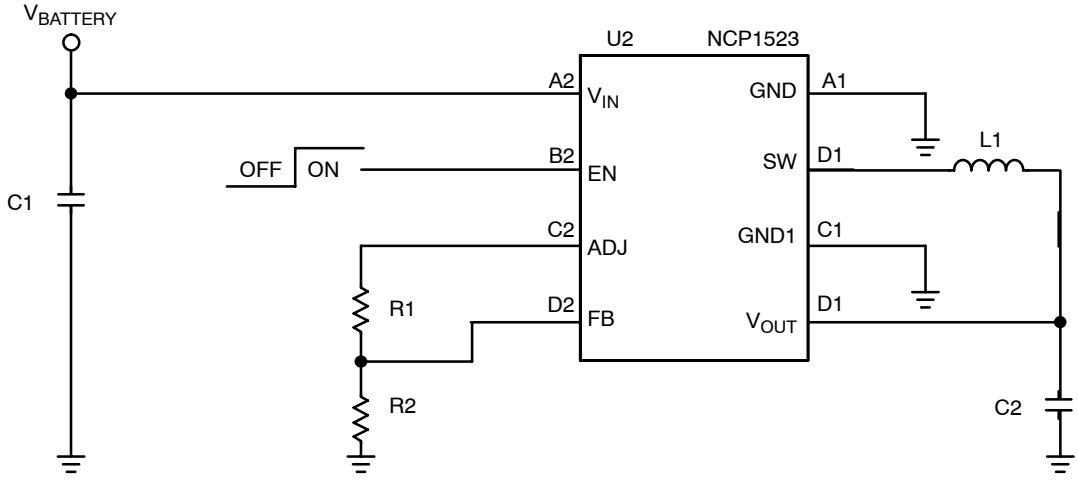


Figure 19. NCP1523 Board Schematic

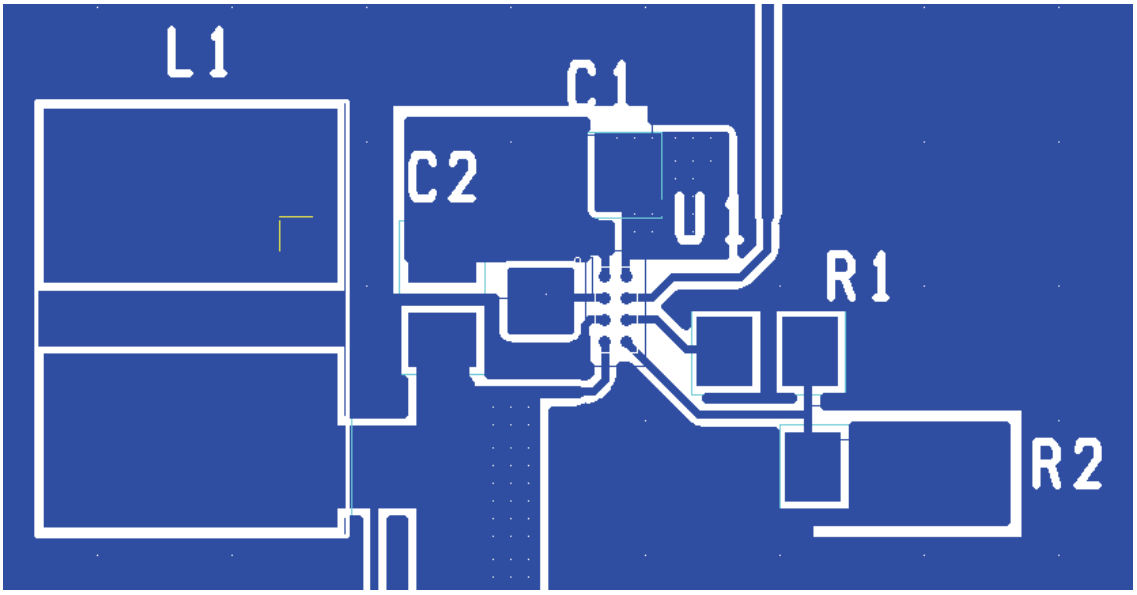


Figure 20. NCP1523 Board Layout

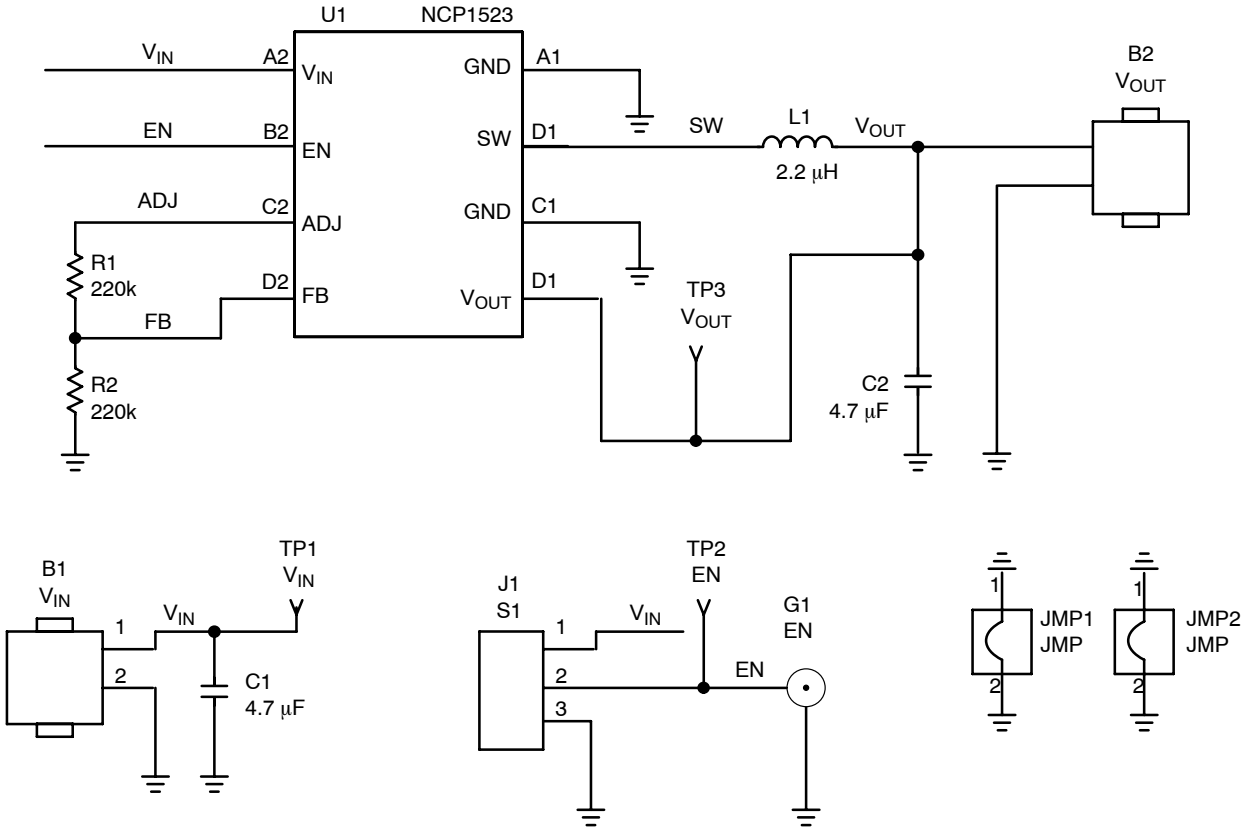


Figure 21. NCP1523 Board Schematic

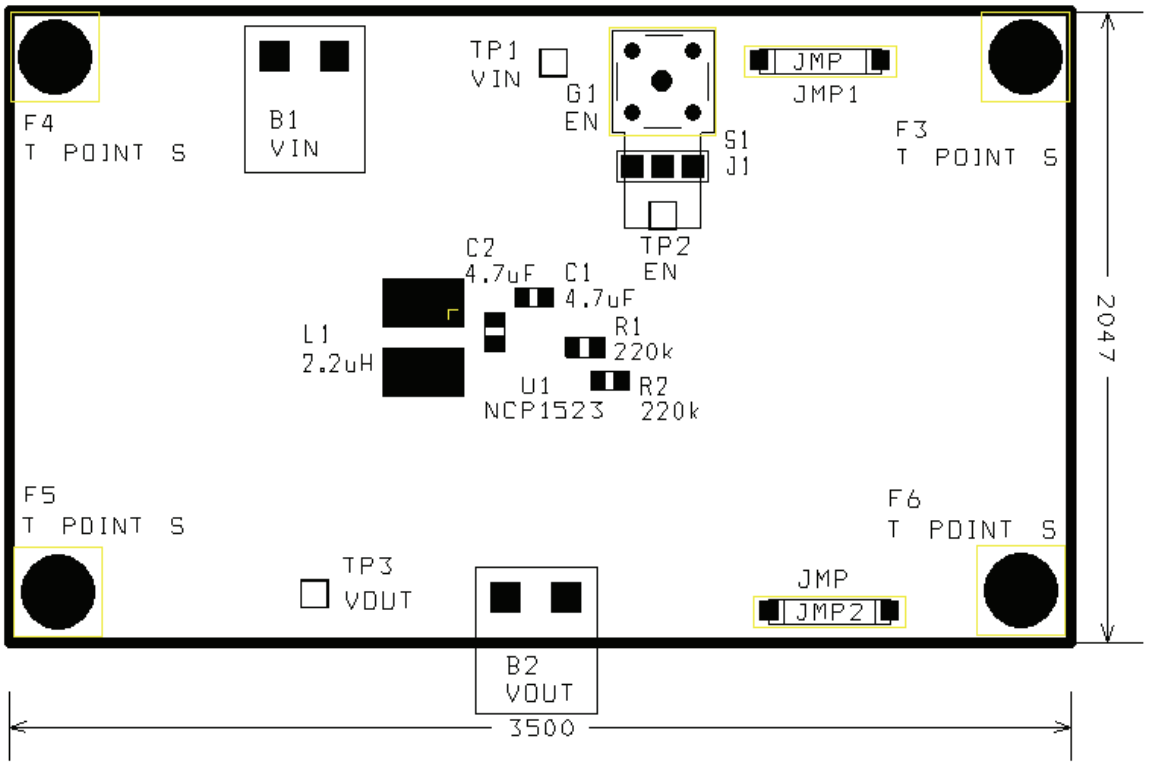


Figure 22. NCP1523 Assembly Layer

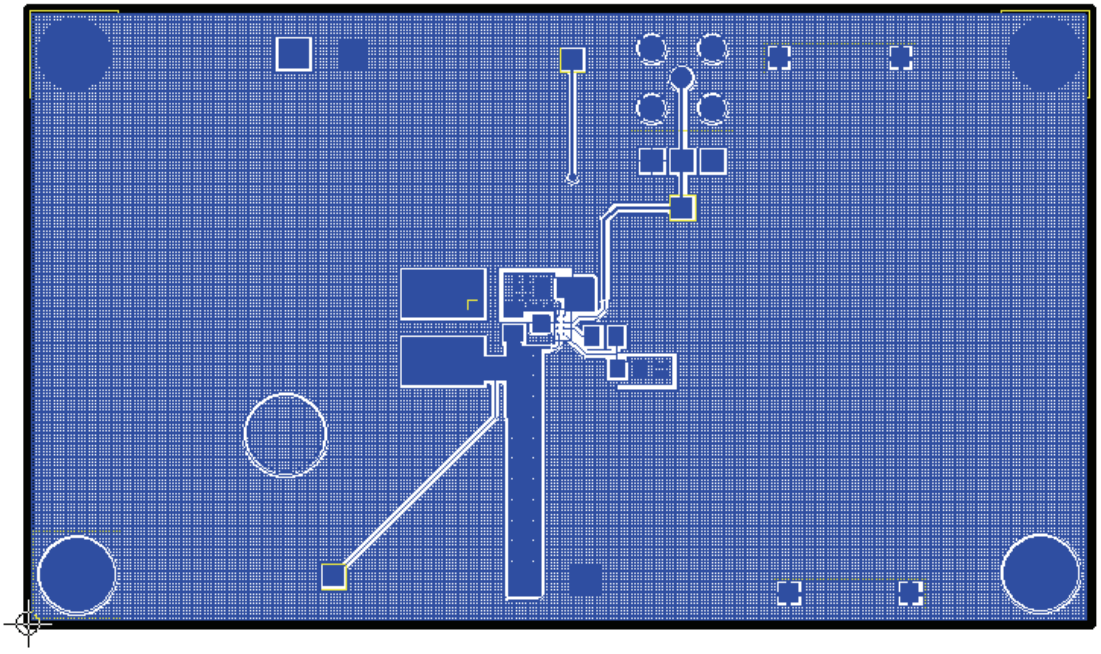


Figure 23. NCP1523 Top Layer Routing

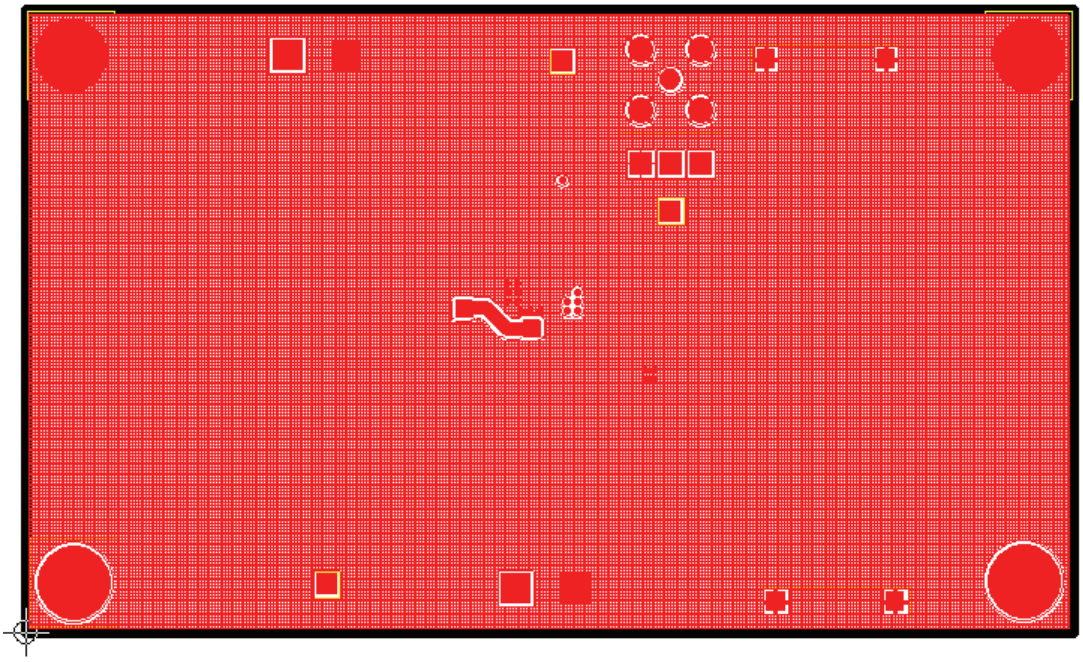


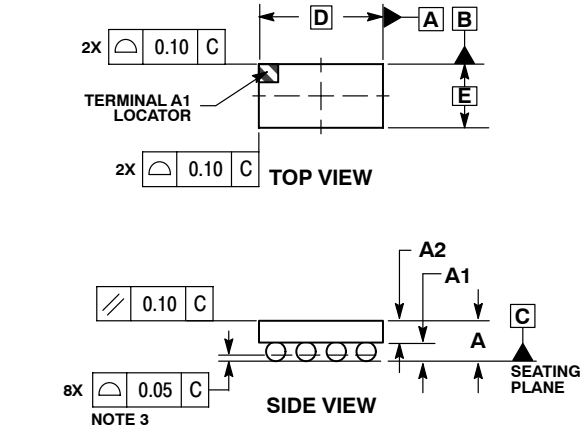
Figure 24. NCP1523 Bottom Layer Routing

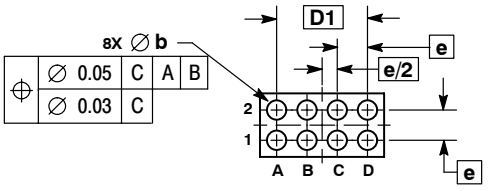
BILL OF MATERIALS

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
U1	1	IC, Converter, DC/DC	NA	NA	8−Pin Flip Chip	ON Semiconductor	NCP1523
C1, C2	2	Ceramic Capacitor	4.7 μF, 10 V, X5R	0,1	0805	Murata	GRM219R61A475 KE19D
R1, R2	2	SMD resistor	220k	0.05	0805	Standard	Standard
L1	1	Inductor	2.2 μH	0.2	1605	Coilcraft	DO1605T−222MLB
B1, B2	2	Male SL5.08/2/90B + Female BLZ5.08/2/90B Connector I/O	NA	NA	NA	Weidmuller	1510360000 + 1555060000
J1	1	3 Pin Jumper Header	NA	NA	2.54 mm	TYCO/AMP	5−826629−0
JMP1, JMP2	2	Jumper for GND	NA	NA	10.16 mm	Harwin	D3082−01
TP1, TP2, TP3	3	Test point	NA	NA	NA	Standard	Standard
G1	0*	SMB Connector	NA	NA	NA	Radiall	R114665000
PCB	1	88.9 x 61.1 x 1.6 mm 4 Layers	NA	NA	NA	Any	TLS−P−001−A−050 6−DA

PACKAGE DIMENSIONS

FLIP−CHIP−8
CASE 766AE−01
ISSUE A





NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.655
A1	0.210	0.270
A2	0.335	0.385
b	0.290	0.340
D	2.050 BSC	
D1	1.500 BSC	
E	1.050 BSC	
e	0.500 BSC	

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NCP1523/D